REMARKS

Claims 1-21, 23, and 27-33 are pending in the present application. Claims 22 and 24-26 were previously canceled. Claim 1 has been amended. No new matter has been added. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

Claims 1, 8, 18, and 23 stand rejected under 35 U.S.C. § 102(b) as assertedly being anticipated by U.S. Publication No. 2005/0189566 to Matsumoto, et al. (hereinafter "Matsumoto"). Claims 2-7, 9-11, 19-21, and 27-31 stand rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Matsumoto. Claims 12-17, 32, and 33 stand rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Matsumoto in view of U.S. Patent No. 5,758,100 to Odisho, et al. (hereinafter "Odisho"). Applicant respectfully traverses these rejections.

Claim 1 requires:

> a first semiconductor device, and
> a second semiconductor device,
> wherein the first semiconductor device and the second semiconductor device each comprise a voltage supply device.

The Examiner has identified items 2A and 2B in Matsumoto as corresponding to the claimed "semiconductor" devices. Office Action at 3. Matsumoto is directed to a "Switching Power-Supply Module" 1 including power conversion circuits, conductor land patterns and conductor terminals that are provided on interconnected circuit boards. Matsumoto at Abstract; Title. Items 2A and 2B are not the semiconductor devices required in claim 1. Instead, Matsumoto clearly identifies items 2A and 2B as "circuit boards" on which electronic components 3 are mounted. Matsumoto at [0004]; Figures 1, 5A and 5B. Electronic components 3 are mounted on the circuit boards 2A and 2B to define switching power-supply circuits. Matsumoto at [0067]. Matsumoto does not teach or suggest that any other non-power-supply components are mounted on circuit boards 2A or 2B.

It is clear from the Matsumoto specification and Figures that circuit boards 2A and 2B are merely parts of a power supply module. Instead, at best, Matsumoto teaches interconnected voltage supply devices formed using components 3 on circuit boards 2A and 2B. An input

power supply 20 and an external load 25 are connected to the Matsumoto power supply module 1. Matsumoto at [0041]. Accordingly, the power supply circuits 3 do not provide power to circuit boards 2A and 2B (the alleged semiconductor devices), but instead provide power to external load 25. Power-supply circuits P_A and P_B provide power to external load 25 either in parallel or in series (i.e. the power output is summed). Matsumoto at [0042], [0058].

> Claim 1 further requires:
>
> wherein the system is adapted such that, in an external access operating mode of the second semiconductor device, the voltage supply device of said second semiconductor device provides the supply voltage for operation of the second semiconductor device, and, in a standby or refresh operating mode of the second semiconductor device, the voltage supply device of said first semiconductor device provides the supply voltage for operation of the second semiconductor device.

The Examiner identifies a power-save or non-operating mode in Matsumoto's paragraph [0039] as anticipating this feature. Office Action at 3. Applicant is unable to find such a disclosure in paragraph [0039]; however, in paragraph [0075], Matsumoto discloses a power-save mode and a non-operating state. A non-operating state is not the same as the claimed "standby or refresh operating mode" that is required in claim 1. The standby or refresh mode in claim 1 is still an operating mode. Conversely, Matsumoto teaches a non-operating state in which one of the power-supply circuits does not operate at all and, instead, the other power supply circuit operates alone. Matsumoto at [0075].

Furthermore, as noted above, Matsumoto's power supply circuits P_A and P_B are merely mounted on circuit boards 2A and 2B, but do not power the circuit boards 2A or 2B. There is no teaching or suggestion in Matsumoto that circuit boards 2A or 2B "operate" or require power at all. Instead, power supply circuits P_A and P_B are designed to provide power to a single external load 25. Even if the external load was a semiconductor device, it is not a first and second semiconductor device as required in the claims.

The Matsumoto reference fails to teach first and second semiconductor devices each comprising a voltage supply device. Furthermore, Matsumoto fails to teach that the voltage supply device of a second semiconductor device provides the supply voltage for operation of the second semiconductor device, or that the voltage supply device of a first semiconductor device

provides the supply voltage for operation of the second semiconductor device. Accordingly, the cited reference does not teach each and every element of the pending claims and, therefore, does not anticipate the claim under 35 U.S.C. § 102(b).

Claims 2-21, 23, and 27-33 depend from claim 1 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicant's attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge, or credit any overpayment, Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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